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(Not for submission under 37 CFR 1.99)

Application Number	10544894
Filing Date	2006-07-19
First Named Inventor	Dasu, Aravind R.
Art Unit	2193
Examiner Name	Bullock Jr, Lewis Alexander Tuan Vu
Attorney Docket Number	117316-155055

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/VAT/	1	Singh, H. et al. " MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications" IEEE Transactions on Computers, 2000	☐
/VAT/	2	Soukup, J. " Fast Maze Router" Proceedings of the 15th Design Automation Conference, pp. 100-102, 1978	☐
/VAT/	3	Strauss, M., et al. "BOPS: Conquering the Geometry Pipeline" Game Developers Conference. March 22-26, 2004, San Jose, California	☐
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/VAT/	12	Zhang, H., et al. " A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing" IEEE Journal of Solid-State Circuits, 35 (11), pp. 1697-1704, November 2000	☐
/VAT/	13	Zhang, H., et al. " Interconnect Architecture Exploration for Low-Energy Reconfigurable Single-Chip DSPs" IEEE Computer Society Workshop on VLSI'99 pp. 2-8, April 1999	☐

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